On-Chip Tap-Delay Measurements for a Digital Delay-Line Used in High-Speed Inter-Chip Data Communications

Octavian Petre, Hans G. Kerkhoff
MESA+ Research Institute
Testable Design and Testing of Microsystems Group
7500AE Enschede, The Netherlands
E-mail: O.Petre@utwente.nl

Abstract

During the last few years, new synchronization techniques to send data between IC’s at increasingly high data-rates have been developed. Some of them rely on digital delay lines. The timing accuracy of the delay lines is crucial for a good functionality of the synchronization mechanism. This paper will present a strategy to measure the tap-delays of a digital delay-line, using the well-known oscillation technique. The occurring measurement error for the presented technique has been calculated. Towards the end of the paper, a new delay-line scheme is shown. The tap-delay measurement becomes much more accurate for this delay-line than for a standard delay-line.

1. Introduction

Nowadays, in order to optimize the entire PCB system, higher data-transfer rates between IC’s are required more than ever. As a result, the clock/data skew can span tens of clock cycles. In order to cope with this new situation, synchronization strategies have been developed [9]. Some of the synchronization techniques rely on a sometimes controllable delay-line [1, 6–8]. The synchronization mechanism, which is based on cross-correlation, is highly dependent on the tap-delays of the delay-line. This paper presents a technique to measure/characterize such tap-delays. It also presents a new delay-line scheme which is better suited for the chosen test-method.

The paper is organized as follows: the next section (2) shows the basic delay-line scheme and also the requirement for the tap-delay measurement tolerance is dealt with. The following section (3), presents the method to be used for measuring the tap-delays. Section 4 shows the simplified scheme used to measure the oscillation periods using the counting technique [4]. The influence of different parameters, such as power supply and temperature, on the measurement tolerance is investigated in section 5. Section 6 presents a new delay-line scheme which is less susceptible to power supply and temperature variations from the testing point of view. Finally, conclusions are given in section 7.

2. The Delay Line

The design of a delay-line for which we intend to measure the tap-delays is presented in figure 1. The measurement accuracy should be ±5%. The intrinsic buffers, $t_{10}$, $t_{21}$, ..., $t_{87}$, are comprised of an even number of inverters, usually 2. Each path, either $X$ (out$^X$) or $Y$ (out$^Y$), has only one enabled output-buffer at any time.

![Figure 1. The delay-line as used in the synchronization mechanism](image)

The initial hardware overhead required to make the circuit testable using the oscillation technique, is shaded in figure 1. Trying to measure any tap-delay with an accuracy of at least 5% is not a trivial task, since the required accuracy
is in the same range as the rising and falling times of the signals involved.

The oscillation-test technique [2, 3] is able to provide the necessary measurement accuracy if the oscillation period is accurately determined. The following sections of the paper will present the basic equations and scheme for measuring the tap-delays using the oscillation technique.

3. Basic Equations for Determining the Tap Delays

The equations (1-2) describe the first step of the method for determining the tap delays. All the notations are depicted in figure 1. The average delay between falling and rising propagation delays from net 'A' to net 'C' is represented by \( t_{\text{err}}^Y \). The other delays in the schematic \( (t_{0}^Y, t_{10}, \ldots) \) represent also the average delays between falling and rising propagation delays. Therefore, from figure 1 one may derive:

\[
t_{\text{err}}^Y + t_{0}^Y = \frac{T_{\text{err}}^Y}{2} \tag{1}
\]

\[
t_{\text{err}}^Y + t_{87} + \ldots + t_{10} + t_{8}^Y = \frac{T_{\text{err}}^Y}{2} \tag{2}
\]

where \( T_{0}^Y \) and \( T_{8}^Y \), denote the oscillation periods when the output-buffers corresponding with the tap number 0 and 8 respectively, are enabled, each at a time. The shaded transmission gate, belonging to the DfT hardware of path \( Y \) in figure 1 is conducting, its transmission gate counterpart of path \( X \) is non-conducting. For path \( X \), the equations can be easily extended. From equations (1) and (2) one can deduce:

\[
T_{1}^Y - T_{0}^Y \overset{\text{def}}{=} T_{10} = 2(t_{10} + t_{1}^Y - t_{0}^Y) \tag{3}
\]

\[
T_{8}^Y - T_{7}^Y \overset{\text{def}}{=} T_{87} = 2(t_{87} + t_{8}^Y - t_{7}^Y) \tag{4}
\]

As can be seen, the term \( t_{\text{err}}^Y \) does not appear in these equations. The additional hardware does therefore not influence the computation of the tap-delays.

The \( T_{0}^Y/2 \) value is in fact the value of the tap-delay between \( \text{tap0} \) and \( \text{tap1} \) at the \( Y \) path access points, and not the intrinsic tap-delay \( (t_{10}) \). From a functional point of view, the tap-delays at the \( Y \) path access points are of more importance than the intrinsic tap-delays, since the signals \( \text{out}^Y \) and \( \text{out}^X \) are the ones used afterwards for the synchronization mechanism. However, in a fault-free situation, one expects \( T_{0}^Y/2 \) to be very close to the \( t_{10} \) value, since the transmission gates and inverters preceding them, which are a source of uncertainty, can be very well matched in the layout.

4. Block Scheme for Measuring the Oscillation Periods

The oscillation periods of the different delay-line sections should be measured in a digital way if a BIST strategy is envisioned. The solution for digitally measuring the period is not new [4]. The block scheme used to perform this operation is shown in figure 2.

![Figure 2. The basic scheme for measuring the tap-delays](image)

The inverter \( U0 \) and the transmission gate \( U1 \) is added in order to make the circuit to oscillate. The \( U2 \) inverter acts as a buffer for the counter which counts the number of rising edges as long as the enable signal \( \text{obs} \) is high. The number stored in the counter will be increased by one on every rising edge of the clock \( \text{clk} \) if \( \text{obs} \) signal is high. From figure 3, it holds:

\[
T_{\text{obs}} \approx N_{1}^Y \cdot T_{1}^Y \tag{5}
\]

\[
T_{\text{obs}} \approx N_{0}^Y \cdot T_{0}^Y \tag{6}
\]

in which:

- \( T_{\text{obs}} \) is the duration when the \( \text{obs} \) signal is high as can be seen in figure 3.

- \( N_{0}^Y \) and \( N_{1}^Y \) denote the numbers stored in the counter when the oscillation periods \( T_{0}^Y \) and \( T_{1}^Y \) are measured.

From equations (3), (5) and (6), the tap-delay \( t_{10} \) is calculated to be:

\[
t_{10} \approx \frac{T_{10}^Y}{2} \approx \frac{T_{\text{obs}}}{2} \frac{N_{0}^Y - N_{1}^Y}{2N_{1}^Y N_{0}^Y} \tag{7}
\]

5. Accuracy of Oscillation Period Measurements

This section deals with the measurement accuracy, using the scheme shown in figure 2. The analysis is impor-
tart because the subsequent digital synchronization mechanism rely on equidistant tap-delay values within a predefined range. Any delay-fault present in the delay-line can disrupt the expected functionality of the synchronization mechanism.

Measuring the oscillation periods requires two steps:

Step 1. After resetting the counter, it will be enabled by the obs signal. Subsequently, the counter will count the number of rising edges of the oscillation period to be measured.

Step 2. When obs becomes low, a number will be stored in the counter. This number is used to calculate the particular oscillation period, using for example equation (5).

As can be seen, finding the value of any oscillation period implies in fact a measurement and a calculation. Hence, during the remaining of the paper the measurement word will mean the first step while the calculated word will indicate the second step.

The main sources of the measurement error can be divided into four categories:

A. digital rounding - this is due to the fact that the oscillation period and the observation time are not correlated.

B. observation time affected by random jitter

C. systematic error when generating the observation time

D. analog parameters - like VDD and Temperature that can vary during adjacent measurement periods.

These four effects will be carefully analyzed in the following subsections.

5.1. Digital Rounding as a Source of Measurement Error

Because the periodic signal of a ring oscillator is not correlated with the observation time ($T_{obs}$), there will always be a measurement error:

$$T_{obs} = N_0^Y \cdot T_0^Y + u \cdot T_0^Y, \quad u \in (-1, 1)$$ (8)

where $u$ is a random variable having an uniform distribution between (-1, 1), and $N_0^Y$ is the number stored in the digital counter. $N_0^Y$ represents the number of rising edges during the time when the enable signal of the counter is high. It should be noted that before every oscillation period measurement, the counter should be reset. In figure 3, two extreme situations for $u$ are shown.

From equation (8), one can infer that the maximum measurement error when calculating $T_0^Y$ is $T_0^Y / N_0^Y$. A simple conclusion could be that by extending the number of bits of the counter, and hence increasing $T_{obs}$, the digital rounding error can be made as small as desired.

Let us consider measuring an oscillation period that has the nominal value $T_0^Y = 25 \times 400$ps with an accuracy of $\pm 20$ps. Therefore $20$ps $\geq T_0^Y / N_0^Y$. Hence $N_0^Y$ $\geq 500$. The observation time should be $T_{obs}$ $\geq 5\mu$s. Keeping the oscillation period as small as possible, will also decrease the observation time, while keeping the absolute measurement accuracy the same. A new delay line scheme will be presented in section (6) which will make use of the observation above.

However, if between adjacent oscillation periods measurements the value of $T_{obs}$ is randomly changing, then the obtained resolution cannot be as small as one would like, but will be dependent on the jitter in $T_{obs}$.

5.2. Observation Time Affected by Jitter

The effect of jitter [5] for our observation time $T_{obs}$ is illustrated in figure 4. The peak-to-peak representation is considered in this figure. "$j^i$" is a random variable having a Gaussian distribution. The $max(|j|)$ value is considered to be at $3\sigma$.

![Figure 3. Measurement error due to digital rounding - two extreme cases for $u$. a) $u = -1$ b) $u = 1$](image)

![Figure 4. The jitter affecting $T_{obs}$](image)

It is further considered that $j_i^Y$ is the jitter value, when one wants to measure the oscillation period $T_i^Y, \ i = 1, 2, \ldots, 8$. The parameter $j_i^Y$ is measured in seconds, and
is within the peak-to-peak jitter range shown in figure 4. \( j_i^Y \) is in fact an event of the \( j \) random variable. Therefore, when measuring \( T_i^Y \), the observation time \( T_{\text{obs}} \) has the following value: \( T_{\text{obs}} + j_i^Y \). Because of the these tiny variations, the measured value of the oscillation periods will be determined with a certain error.

The value of the observation time affected by jitter when measuring the oscillation period \( T_i^Y \) will be denoted \( T_{\text{obs}i} \). The values, \( T_{\text{obs}i} \), when \( i = 1, 2, \ldots, 8 \), are different for each measurement but the average value is \( T_{\text{obs}} \).

By definition \( h_i^Y \) is defined as:

\[
 h_i^Y = \frac{j_i^Y}{T_{\text{obs}}} \quad (9)
\]

Hence, the influence of the jitter on the observation time, when measuring the oscillation period \( T_i^Y \), is given by:

\[
 T_{\text{obs}i}^Y = T_{\text{obs}}(1 + h_i^Y), \quad i = 1, 2, \ldots, 8 \quad (10)
\]

It is further denoted with \( N_i^Y \), the value stored in the counter, as a result of the \( T_i^Y \) oscillation period measurement, while having an observation time \( T_{\text{obs}i} \) affected by jitter. Rewriting equation (8), replacing \( T_{\text{obs}} \) with \( T_{\text{obs}i} \), \( N_i^Y \) with \( N_i^Y \) and \( T_i^Y \) with \( T_{\text{obs}i}^Y \), results in:

\[
 T_{\text{obs}i}^Y = N_i^Y T_i^Y + uT_i^Y, \quad u \in (-1, 1) \quad (11)
\]

The value calculated for \( T_{\text{obs}i}^Y \), which will be denoted \( T_{\text{obs}i}^{Y \text{calculated}} \), is in fact: \( T_{\text{obs}}/N_i^Y \) since there is knowledge of \( T_{\text{obs}} \) and \( N_i^Y \) (value stored in the counter).

Therefore \( T_{\text{obs}}^{Y \text{calculated}} \), using equation (11), can be expressed as:

\[
 T_{\text{obs}}^{Y \text{calculated}} = \frac{T_{\text{obs}}}{N_i^Y} = \frac{T_i^Y T_{\text{obs}}}{T_{\text{obs}i}^Y - uT_i^Y} \quad (12)
\]

Hence the difference between the exact value of any oscillation period(\( T_i^Y \)) and the calculated one is:

\[
 T_{i}^{Y \text{calculated}} - T_i^Y = T_i^Y \left( \frac{T_{\text{obs}} - T_{\text{obs}i} + uT_i^Y}{T_{\text{obs}i}^Y - uT_i^Y} \right) \quad (13)
\]

The above expression represents the error measurement for \( T_i^Y \) in picoseconds. A percentage representation is much more illustrative and is obtained by dividing equation (13) with \( T_i^Y \). Denoting the result with \( l_i^Y \), which represents the measurement error in percentage, and replacing \( T_{\text{obs}i} \) using (10), it can be derived:

\[
 l_i^Y = \frac{-T_{\text{obs}}h_i^Y + uT_i^Y}{T_{\text{obs}}(1 + h_i^Y) - uT_i^Y} \quad (14)
\]

In the above equation, \( l_i^Y \) should be as small as possible. Hence, the worst case value for \( l_i^Y \), is when \( u = 1, h_i^Y \) is negative and \(|h_i^Y|\) is maximum. Defining \( h = \max|h_i^Y| \) and \( l = l_i^Y_{\text{worst case}} \) it can be stated:

\[
 l = \frac{\max h_i^Y}{T_{\text{obs}}(1-h) - T_i^Y} \quad (15)
\]

Two limiting cases may be identified in (15):

1. \( T_{\text{obs}}h \ll T_i^Y \) - This is the particular case discussed in subsection 5.1, when there was no jitter within the observation time. In this case "\( h \)" can be decreased by increasing the \( T_{\text{obs}} \). For a very low jitter clock one can realize a small measurement error.

2. \( T_{\text{obs}}h \gg T_i^Y \) - In this case "\( l \)" may be approximated with: \( l = h/(1-h) \) and this is common for large and jittery observation times. For small values of "\( h \)" and this is always the case, it can be inferred that \( l \approx h \). Hence, the smallest measurement error for the oscillation periods is "\( h \)".

The values of the subsequent tap oscillation periods have increasing values, while the absolute accuracy to measure them remains the same. Hence, measurement of \( T_{8}^Y \) demands the lowest jitter requirements on \( T_{\text{obs}} \).

Now let us consider that one wants to measure the oscillation period \( T_{8}^Y = 25 \times 400 \text{ps} \) with an accuracy of at least \( \pm 20 \text{ps} \). This is equivalent of having an accuracy \( \leq 0.2\% \). If the observation time, \( T_{\text{obs}} \), is sufficiently large then the second limiting case should be considered. In this case the accuracy of measuring \( T_{8}^Y \) is \( l \approx h \). Therefore \( h \leq 0.2\% \), which in turn requires a maximal peak-to-peak value of jitter \( 2 \cdot \max(|j|) = 2 \cdot 0.2\% \cdot T_{\text{obs}} \) (see figure 4 and relation (9)).

### 5.3. Systematic Error When Generating the Observation Time

Another source of uncertainty when measuring the oscillation periods, is the systematic error of the generated frequency used as the enable signal for the counter in figure 2. If one defines the percentage of the systematic error of the generated frequency with \( k \), then it can be written:

\[
 T_{\text{obs generated}} = T_{\text{obs}}(1 + k) \quad (16)
\]

\( T_{\text{obs generated}} \) is the observation time generated by the frequency generator. \( k \) is constant during all the measurements of the taps.

It can be shown that the measurement error for any oscillation period is the same as the systematic error \( k \) for the generated frequency. Usually \( k \) is less than 1\%. Hence, \( k \) does not significantly influence the oscillation periods measurements since the accuracy needed is \( \pm 5\% \).

All the sources of error presented above - digital rounding, jitter, generated observation time error - should be
added together in order to find the total oscillation-period measurement-error. The next sections present the influence of power-supply (VDD) and temperature on the measurement-error.

5.4. Power-supply and Temperature Variations Requirements

5.4.1 Power-supply Variations

It is well known that the power supply (VDD) has a direct influence on the oscillation period of inverter-based oscillators. In this subsection, variations of $T_i^Y$, $i = 0, 2, \ldots, 8$, with VDD will be investigated.

The drift of the oscillation period, due to the power-supply variation during adjacent measurements, which can be seen as a measurement error for $T_i^Y$, should be smaller than an accepted error $t_{\text{accepted error}}$ as stated below:

$$\frac{dT_i^Y}{dVDD}_{VDD_{i-1}} \cdot (VDD_i^Y - VDD_{i-1}^Y) \leq t_{\text{accepted error}}$$

where $VDD_i^Y$ is the power-supply voltage at the moment the oscillation period $T_i^Y$ is measured.

From equation (17), the restriction on VDD variations between adjacent measurement periods can be derived:

$$\Delta VDD \leq \frac{t_{\text{accepted error}}}{\frac{dT_i^Y}{dVDD}_{VDD_{i-1}}}$$

where $\Delta VDD = VDD_i^Y - VDD_{i-1}^Y$.

Let us presume that $t_{\text{accepted error}} = 10\text{ps}$ and $VDD_i^Y = 1.8\text{V}$. From simulations of our delay-line in HSPICE, one can find that $\frac{dT_i^Y}{dVDD}_{VDD_i^Y=1.8}\text{V} = 4 \times 10^{-9}[s/V]$. Therefore, $\Delta VDD \leq 2.5\text{mV}$.

As can be seen, the requirement on the power-supply is high. In section 6, a new delay-line scheme is presented which relaxes the VDD requirement. However, a voltage stabilized source is still needed.

5.4.2 Temperature Variations

Similar to the power-supply calculations, the restriction on temperature (Temp) variations between adjacent period measurements can be derived to be:

$$\Delta Temp \leq \frac{t_{\text{accepted error}}}{\frac{dT_i^Y}{dTemp}_{Temp_{i-1}^Y}}$$

where $\Delta Temp = Temp_i^Y - Temp_{i-1}^Y$ and $Temp_i^Y$ is the chip temperature when the oscillation period $T_i^Y$ is measured.

From HSPICE simulations of our delay-line it was found that: $\frac{dT_8^Y}{dTemp}_{Temp_i^Y} = 1.91 \times 10^{-11}[s/\text{C}]$. Allowing $t_{\text{accepted error}} = 10\text{ps}$, it can be inferred that $\Delta Temp \leq 0.52\text{C}$.

As can be seen, the temperature and VDD variations during measurements play a vital role when determining the oscillation periods, and therefore the tap delays. If the power supply and/or temperature variations are too high for the accepted measurement tolerance, then a redesign of the delay line should be carried out. A possible implementation of such a delay line is presented in section 6.

6. A New Delay-Line Design Featuring a Higher Measurement Accuracy

As was seen in the previous sections, the main disadvantage of the initial design is the increase of the oscillation period while the absolute value of the measurement error remains the same. The new delay-line design, shown in figure 5, is able to connect any feed-back signal anywhere within the delay-line.

![Figure 5. New delay-line scheme for higher measurement accuracy](image-url)

In the scheme, two new oscillation loops $T_{7-6}^X$ and $T_{8-6}^X$ are shown. This particular configuration is used for determining the tap-delay $t_{87}$. The susceptibility to power-supply and temperature has been decreased for this tap.

For the new scheme in figure 5, the signal $obs$, shown in figure 2, has the same value for all oscillation-period measurements. This is the case because the values of the oscillation periods are in the same range. This significantly simplifies its generation procedure. By decreasing the oscillation periods, the test time is reduced, because the test
time is quadratically dependent on the oscillation period, $T_{obs} \sim (T_i)^2$ for a certain measurement accuracy.

Table 1 shows a comparison between the initial and the new delay-line design for an accepted measurement error of $t_{\text{accepted error}} = 10\,\text{ps}$. The values in the table are derived from simulations in HSPICE using a 0.18$\mu$m UMC process. The test time represents only the observation time for a certain measurement accuracy. With the new delay-line presented in figure 5 it is possible to measure two oscillation periods in parallel; one on each path. For example, it is possible to carry out the measurements of $T_{k-6}^X$ and $T_{i-2}^X$ in parallel. The values of $\Delta \text{VDD}$ and $\Delta \text{TEMP}$ in table 1 are quite small. The following paragraphs will prove that these constraints can be met.

### 6.1. The $\Delta \text{VDD}$ and $\Delta \text{TEMP}$ requirement

Corner simulations have been carried out in order to find the maximum current difference between adjacent measurements drained from the power supply. This value is well within 10mA for a 0.18$\mu$m UMC technology. Knowing that the maximum $\Delta \text{VDD}$ allowed should be less than 4.3mV, it can be concluded that the output dynamic resistance of the power supply should be less than 430 m$\Omega$. There are commercial voltage references which can provide a value almost 10 times lower than the one required above. However the layout resistance of the power supply metal lines, together with the contact resistance and the output resistance of the voltage reference should not exceed 430 m$\Omega$.

Table 1 presents the maximum temperature deviation allowed for a measurement error of 10ps. Because the oscillation frequency of the ring oscillators is quite high, around 0.5GHz, the self-heating of the IC could influence the measurements. Calculation of the necessary Junction-to-Ambient ($\Theta_{JA}$), in order not to have a higher $\Delta \text{TEMP}$ as a result of self-heating, was carried out. The value of $\Theta_{JA}$ should be higher than 59.26 $^\circ$C/W. Most of the packages can provide this value. Hence, both requirements can be met.

### 7. Conclusions

In this paper, a method for measuring the tap-delays of a digital delay line used for high-speed data synchronization is presented. By measuring the taps-delays, it is possible to pinpoint where delay-faults and/or stuck-at-faults are located. It has also been shown which design equations are to be considered in order to find the measurement accuracy of the tap-delays. These equations can be extended for other oscillation-based testing techniques which use a digital counter for finding the oscillation period. For obtaining a higher measurement accuracy, a new delay-line design was presented, which is capable of reducing the test time and the influence of analogue parameters like power-supply and temperature variations.

### References


